REMARKS/ARGUMENTS

This Response to Office Action is responsive to the Office Action dated June 14, 2005. Applicants respectfully request further examination and reconsideration in view of the arguments set forth fully below. Claims 1-12, 14-22, 24-32, 34-39, and 42-51 were previously pending in this application. Claims 1-12, 14-22, 24-32, 34-39, 42-43 and 48, have been rejected. Claims 31-32 and 49-50 have been objected. By the above amendments, Claims 1, 5, 9, 14-19, 22, 24-29, 31-32, 34, 36-37, 39, 43-45, 47-49 and 51 have been amended. Claims 44-47 and 51 have been allowed. No new matter has been added. Accordingly, Claims 1-12, 14-22, 24-32, 34-39, and 42-51 are now pending in this application.

Claim Objections

The Office Action states that Claims 31 and 32 are objected because of the incorrect spelling of claim in line 1 of both claims. Claims 31 and 32 have been amended accordingly.

Rejections under 35 U.S.C. § 103

Within the Office Action, Claims 1, 3-5, 7-8, 34, 36, 38-39, and 48 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,828,255 to Kelkar et al. (hereinafter "Kelkar") in view of U.S. Patent No. 5,268,655 to Dong (hereinafter "Dong"). The applicants respectfully disagree with this rejection.

Within the Office Action, Claims 2, 6, and 35 have been rejected under 35 U.S.C. § 103(a) as being unpatentable Kelkar in view Dong, and in further view of U.S. Patent Application No. 2002/0064247 to Ahn et al. (hereinafter "Ahn"). The applicants respectfully disagree with this rejection.

Within the Office Action, Claims 9, 10, 14-17, 19, 20, 26-27, 29, and 32 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelkar in view of Dong. The applicants respectfully disagree with this rejection.

Newly Cited Art

Dong teaches an automatic phase-locked loop (hereinafter "PLL") parameter adjusting device and a method for automatically adjusting PLL parameters. [Dong, col. 1, lines 62-65] Dong teaches a method for automatically adjusting parameters of a PLL that has a PLL error output signal. The method comprises successively integrating the PLL output signal over N samples to provide a sum. N is a first preselected integer and provides a pluarlity of sums. K sums are checked where K is a second preselected integer. Each sign of the sum is recorded and counted. The counted record is compared to a predetermined threshold value. The PLL and N parameters are adjusted according to a predetermined strategy based on the comparison. [Dong, col. 2, lines 33-46] The predetermined strategy is used to automatically adjust the parameters of the PLL to either accelerate or decelerate the PLL tracing speed. [Dong, col. 8, lines 20-36]

Dong does not teach to measure relative jitter between a recovered clock and recovered data and to adjust the PLL loop bandwidth of the receiver to reduce the relative jitter. Rather, Dong teaches to compare a counter signal to a predetermined threshold value in order to adjust N (the sample interval) and the PLL parameter values in order to accelerate or decelerate the PLL tracking speed. [Dong, col. 8 lines 3-37] Further, Dong does not teach a phase pointer determined from an integration of the magnitude of an AC component of a control voltage. Rather, Dong teaches a hard-limiting circuit operably coupled to receive a sum signal over a predetermined number of samples. [Dong, col. 3, lines 17-20; col. 4 64-66]

Ahn teaches a high-speed CMOS technique. Ahn teaches a communication system utilizing a gigabaud CMOS driver which include a receiver with on-chip termination to significantly reduce distortion in the presence of parasitic capacitance in inductance in comparison to a receiver with external termination. [Ahn, 0009] Further, Ahn teaches a finder to determine the most frequent transition-edge in the contents provided by a D-type flip flop. [Ahn, 0058]

Ahn does not teach that jitter is represented by the activity of a phase pointer. Rather, Ahn teaches that the most frequent transition edge information keeps track of

the sender's clock. [Ahn, 0058]

Newly Cited Art Distinguished

Claims 1, 3-5, 7-8, 34, 36, 38-39, and 48

In contrast to Dong, Claim 1 includes the language "measuring phase pointer activity where a phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver" and "adjusting the PLL loop bandwidth of the receiver to reduce the relative jitter." Dong teaches to compare a counter signal to a predetermined threshold value. Further, Dong teaches to adjust the sample interval and the PLL parameter values according to the results of the comparison in order to change the tracking speed of the PLL. [Dong, col. 8, lines 3-37] Thus, Dong does not teach "measuring phase pointer activity where a phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver" and "adjusting the PLL loop bandwidth of the receiver to reduce the relative jitter." Therefore, Dong does not render Claim 1 unpatentable. For at least these reasons, the independent Claim 1 is allowable over the teachings of Dong.

Claims 2-4 are directly dependent on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Dong. Accordingly, Claims 2-4 are also at least allowable as being dependent on an allowable claim.

Claim 5 includes the language "means for measuring phase pointer activity where a phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver" and "means for adaptively adjusting the PLL loop bandwidth of the receiver to reduce the relative jitter." Since Dong does not teach "means for measuring phase pointer activity where a phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver" and "means for adaptively adjusting the PLL loop bandwidth of the receiver to reduce the relative jitter," Dong does not render Claim 5 unpatentable. For at least these reasons, the independent Claim 5 is allowable over the teachings of Dong.

Claims 6-8 are directly dependent on the independent Claim 5. As described

above, the independent Claim 5 is allowable over the teachings of Dong. Accordingly, Claims 6-8 are also at least allowable as being dependent on an allowable claim.

Claim 34 includes the language "phase pointer representing a relative jitter between the recovered data and clock" and "wherein a loop bandwidth of the PLL can be adjusted based on the control signal from the control logic." Since Dong does not teach "phase pointer representing a relative jitter between the recovered data and clock" and "wherein the loop bandwidth of the PLL can be adjusted based on the control signal from the control logic," Dong does not render Claim 34 unpatentable. For at least these reasons, the independent Claim 34 is allowable over the teachings of Dong.

Claims 35-38 are directly dependent on the independent Claim 34. As described above, the independent Claim 34 is allowable over the teachings of Dong. Accordingly, Claims 36-38 are also at least allowable as being dependent on an allowable claim.

Claim 39 includes the language "to minimize the relative phase between a recovered data and clock where the receiver and a transmitter operate at substantially the same clock frequency." Since Dong does not teach "to minimize the relative phase between a recovered data and clock where the receiver and a transmitter operate at substantially the same clock frequency," Dong does not render Claim 39 unpatentable. For at least these reasons, the independent Claim 39 is allowable over the teachings of Dong.

Claims 42-43 are directly dependent on the independent Claim 39. As described above, the independent Claim 39 is allowable over the teachings of Dong. Accordingly, Claims 42-43 are also at least allowable as being dependent on an allowable claim.

Claim 48 includes the language "receiver has a phase-locked loop (PLL) with a loop bandwidth for recovering the clock and data from the transmitter" Since Dong does not teach "receiver has a phase-locked loop (PLL) with a loop bandwidth for recovering the clock and data from the transmitter," Dong does not render Claim 48 unpatentable. For at least these reasons, the independent Claim 48 is allowable over

the teachings of Dong.

Claims 2, 6, and 35

As recited above, Claims 2-4 are directly dependent on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Dong. Accordingly, Claims 2-4 are also at least allowable as being dependent on an allowable claim.

Claim 2 includes the language "relative jitter is represented by the activity of a phase pointer." Ahn teaches a finder that determines the most frequent transition-edge in order to keep track of the sender's clock. Thus, Ahn does not teach "relative jitter is represented by the activity of a phase pointer." Therefore, Ahn does not render Claim 2 unpatentable. For at least these additional reasons, Claim 2 is allowable over the teachings of Ahn.

As recited above, Claims 6-8 are directly dependent on the independent Claim 5. As described above, the independent Claim 5 is allowable over the teachings of Dong. Accordingly, Claims 6-8 are also at least allowable as being dependent on an allowable claim.

Claim 6 includes the language "relative jitter is represented by the activity of a phase pointer indicating a correct data sampling point." Since Ahn does not teach "relative jitter is represented by the activity of a phase pointer indicating a correct data sampling point," Ahn does not render Claim 6 unpatentable. For at least these additional reasons, Claim 6 is allowable over the teachings of Ahn.

As recited above, Claims 35-38 are directly dependent on the independent Claim 34. As described above, the independent Claim 34 is allowable over the teachings of Dong. Accordingly, Claims 36-38 are also at least allowable as being dependent on an allowable claim.

Claim 35 includes the language "oversampling the received data to produce oversampled points from which the phase pointer is selected." Since Ahn does not teach "oversampling the received data to produce oversampled points from which the phase pointer is selected," Ahn does not render Claim 35 unpatentable. For at least

these additional reasons, Claim 35 is allowable over the teachings of Ahn.

Claims 9, 10, 14-17, 19, 20 26-27, 29, and 32

Claim 9 includes the language "phase pointer is determined from integration of a magnitude of an AC component of a control voltage." Dong teaches teaches a hard-limiting circuit operably coupled to receive a sum signal over a predetermined number of samples. [Dong, col. 3, lines 17-20; col. 4 64-66] Thus, Dong does not teach "phase pointer is determined from integration of a magnitude of an AC component of a control voltage." Therefore, Dong does not render Claim 9 unpatentable. For at least these reasons, the independent Claim 9 is allowable over the teachings of Dong.

Claims 10-12 and 14-18 are directly dependent on the independent Claim 9. As described above, the independent Claim 9 is allowable over the teachings of Dong. Accordingly, Claims 10-12 and 14-18 are also at least allowable as being dependent on an allowable claim.

Claim 19 includes the language "a phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver, wherein said phase pointer is determined from integration of a magnitude of an AC component of a control voltage" Since Dong does not teach "the phase pointer represents relative jitter between the recovered clock and the recovered data at the receiver, wherein said phase pointer is determined from integration of a magnitude of an AC component of a control voltage," Dong does not render Claim 19 unpatentable. For at least these reasons, the independent Claim 19 is allowable over the teachings of Dong.

Claims 20-22 and 24-28 are directly dependent on the independent Claim 19. As described above, the independent Claim 19 is allowable over the teachings of Dong. Accordingly, Claims 20-22 and 24-28 are also at least allowable as being dependent on an allowable claim.

Claim 29 includes the language "tracking a phase pointer representing a relative jitter between the recovered data and clock, wherein the data is encoded using Transition Minimized Differential Signaling (TMDS); measuring activity of the phase pointer; and adjusting a loop bandwidth of the receiver PLL based on the phase pointer

activity measured." Since Dong does not teach "tracking a phase pointer representing a relative jitter between the recovered data and clock, wherein the data is encoded using Transition Minimized Differential Signaling (TMDS); measuring activity of the phase pointer; and adjusting a loop bandwidth of the receiver PLL based on the phase pointer activity measured," Dong does not render Claim 29 unpatentable. For at least these reasons, the independent Claim 29 is allowable over the teachings of Dong.

Claims 30-32 are directly dependent on the independent Claim 29. As described above, the independent Claim 29 is allowable over the teachings of Dong. Accordingly, Claims 30-32 are also at least allowable as being dependent on an allowable claim.

Claims 11-12, 21-22, 24, 25, 30-31

As recited above, Claims 10-12 and 14-18 are directly dependent on the independent Claim 9. As described above, the independent Claim 9 is allowable over the teachings of Dong. Accordingly, Claims 10-12 and 14-18 are also at least allowable as being dependent on an allowable claim.

As recited above, Claims 20-22 and 24-28 are directly dependent on the independent Claim 19. As described above, the independent Claim 19 is allowable over the teachings of Dong. Accordingly, Claims 20-22 and 24-28 are also at least allowable as being dependent on an allowable claim.

As recited above, Claims 30-32 are directly dependent on the independent Claim 29. As described above, the independent Claim 29 is allowable over the teachings of Dong. Accordingly, Claims 30-32 are also allowable as being dependent on an allowable claim.

Claims 18 and 28

As recited above, Claims 10-12 and 14-18 are directly dependent on the independent Claim 9. As described above, the independent Claim 9 is allowable over the teachings of Dong. Accordingly, Claims 10-12 and 14-18 are also at least allowable as being dependent on an allowable claim.

As recited above, Claims 20-22 and 24-28 are directly dependent on the independent Claim 19. As described above, the independent Claim 19 is allowable over the teachings of Dong. Accordingly, Claims 20-22 and 24-28 are also at least allowable as being dependent on an allowable claim.

Since Kelkar and Dong are the primary references used to reject Claims 18 and 28, analysis of Dinh is considered to be unnecessary.

Allowable Claims

The applicants have amended Claim 49 to be written in independent form including all the limitations of the base claim. Claim 50 is dependent on Claim 49. No new matter has been added. As such, Claims 49 and 50 are now in condition for allowance.

CONCLUSION

No new subject matter has been added by way of the above amendments. For the reasons given above, the applicants respectfully submit that Claims 1-12, 14-22, 24-32, 34-39, and 42-51 are now in a condition for allowance. The applicant respectfully requests that all rejections be withdrawn and the application be allowed at the earliest date possible. Should the Examiner have any questions or comments, he is encouraged to call the undersigned at (650) 838-4305 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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